REMARKS

Claims 1-18 were the in application. Claims 3-5, 10-12 and 18 were objected to but indicated as allowable over the cited art.

Applicant has amended the specification to more specifically call out the acronym definitions as requested by the Examiner. No new matter has been added.

Applicant has rewritten claims 3-5, 10-12 and 18 to remove the dependency upon a rejected base claim, and such claims should now be in condition for allowance.

As for the rejections of the remaining claims in view of Uchihori and Hussain (whether or not combined with other references), Applicant respectfully traverses these rejections, although to expedite prosecution Applicant has chosen to further amend the independent claims to further amplify distinctions over the cited references.

The independent claims now more expressly recite that the control circuit selectively controls operation of the first and second translation lookaside buffers to selectively output a physical address based on stored enable information, and the control circuit includes storage for storing the stored enable information and a selector coupled to outputs of the first translation lookaside buffer and the second translation lookaside buffer, and the selector selectively operates to output the physical address based on the stored enable information, and upon reset of the date processor the stored enable information controls the selector so that it does not output any physical address from either the first translation lookaside buffer or the second translation lookaside buffer (see, e.g., Applicant's specification at page 7, lines 12-22 and page 9, lines 11-24 for exemplary support; no new matter has been added). Such structure and operation is neither disclosed in nor suggested by the cited references, either alone or in combination.

As previously explained, in accordance with the present invention, first and second TLBs (translation lookaside buffers) are provided in the processor (or in the design data module for the processor, etc.). As described in detail in Applicant's specification, first and second TLBs are utilized in Applicant's invention for more efficient and flexible address translation. A control circuit is provided, and the control circuit selectively controls operation of the first and second translation lookaside buffers to selectively output a physical address based on stored enable information.

Applicant submits that the invention as defined in the presently presented claims amply distinguishes over the set associative structure disclosed in the Uchihori reference and the other cited art. Uchihori discloses a single TLB structure of the so-called 2 way set associative configuration, which is not controlled in the manner described and claimed by Applicant. Although the TLB of the well-known set associative configuration is structured to have a plurality ways (in Uchihori, there are two, designed side A and side B, etc.), this is fundamentally different from a plurality of TLBs as in Applicant's invention, and the control thereof is decidedly different (as was discussed at the interview and as is reflected in the amended claims). Applicant's claims as defined by the claims herein amply distinguish over Uchihori's set associative structure – Uchihori's set associative structure does not structurally or operationally satisfy what is required by Applicant's claims, and such rejection should be withdrawn.

The rejections in view of Hussain similarly should be withdrawn. Hussain does not disclose the use of stored enable information to selectively control the operation of multiple TLBs. Instead, Hussain discloses an operationally and structurally different arrangement by which <u>each memory request</u> includes a virtual address <u>and</u> a descriptor ID. The descriptor ID is used as an index to a TLB descriptor table. Using the descriptor ID included with each memory request, the memory request unit selects a TLB descriptor from the TLB descriptor table. The TLB descriptor selects a segment of the TLB. See, e.g., Hussain col. 2, lines 29-50.

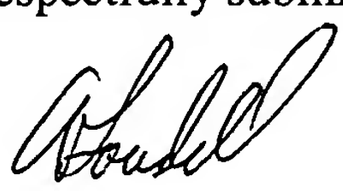
Hussain thus should be understood to expressly teach away from Applicant's use of stored enable information selectively controlling the operation of multiple TLBs. Hussain relies on a descriptor ID that must be included with each memory request ("[e]ach request includes a virtual address and a descriptor ID", col. 2, lines 34-35), a distinctly different way of controlling the TLB in Hussain as compared to that of Applicant's invention. Thus, particularly as defined in the presently submitted claims, Applicant submits that its invention patentably distinguishes over Hussain, whether or not combined with the other references.

Applicant further notes that Applicant's invention also enables selective activation of the TLBs, which can be advantageously used to control power consumption (as in new claims 19 and 20), which would seem not possible based on the structures and operations of Uchihori and Hussain..

Based on the foregoing, Applicant submits that the application is in condition for allowance, and such is respectfully requested. If there are any questions, Applicant's attorney requests an opportunity to discuss such questions with the Examiner by way of a telephone or in-person interview. Reconsideration and allowance is requested.

Please charge any additional fees due, or credit any overpayment, to Deposit Account No. 50-0251.

Respectfully submitted,



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